DE-FE0031972

Reversible SOFC-SOEC Stacks Based on Stable Rare-Earth Nickelate Oxygen Electrodes

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FECM/NETL Spring R&D Project Review Meeting, April 23-25, 2024

REVERSIBLE SOFC-SOEC STACKS BASED ON STABLE RARE-EARTH NICKELATE OXYGEN ELECTRODES: DE-FE0031972

Objectives to be reached during this project

1. Establish state-of-the-art oxygen electrode materials
2. Stabilize Ni-YSZ hydrogen electrode against Ni migration - utilize infiltration
3. Quantify the effect of cell & stack design on durability
4. Develop and quantify cost-effective and scalable manufacturing

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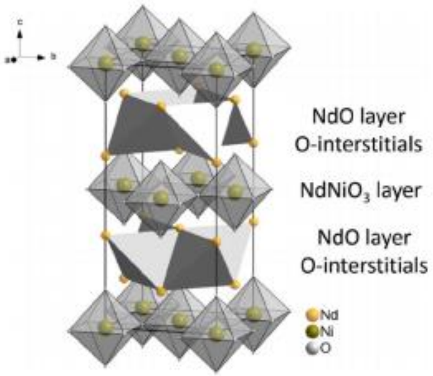
Grant Program Activity	Budget Federal	Budget Non-Federal	Total
Budget Period 1	$796,976	$203,754	$1,000,730
Budget Period 2	$798,961	$197,689	$996,650
Budget Period 3	$794,730	$196,226	$990,956
Totals	**$2,390,667**	**$597,669**	**$2,988,336**

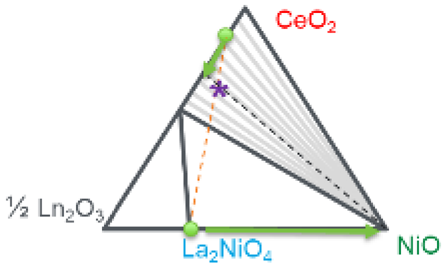
Acknowledgement

NATIONAL ENERGY TECHNOLOGY LABORATORY

Ln_2NiO_4 Air Electrode



Performance Potential



Stability Challenge

FOCUS ON STACK AND REVERSIBLE OPERATION MODE ISSUES

SOLUTIONS AT EACH LEVEL DESIGNED TO BE PORTABLE TO MANY SYSTEM CONFIGURATIONS

Cell Level

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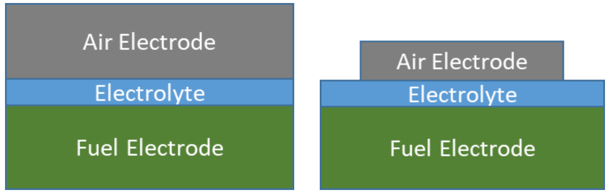
Oxygen Electrode (Nickelates)



Stack Supported | Anode Supported

Fuel Electrode (Nickel migration)

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Stack Level

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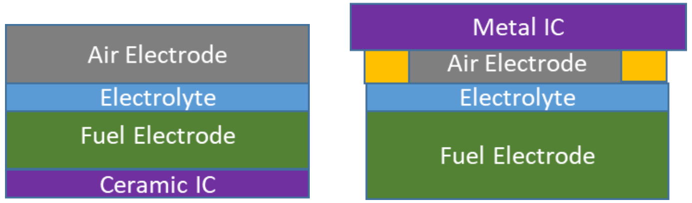
Nickelate – Cr interconnect interactions



Stack Supported | Anode Supported

Ceramic IC humidity interactions

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Scale Up

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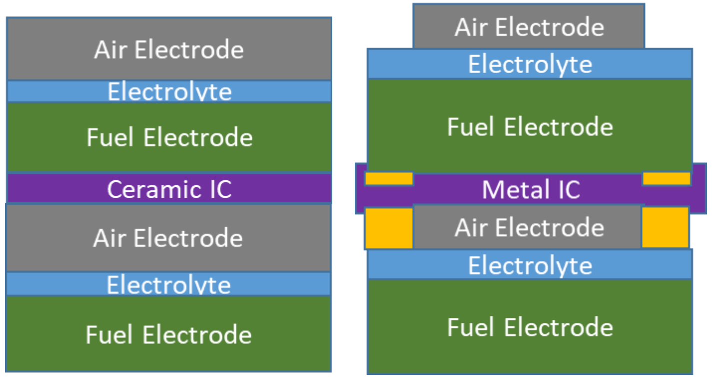
Solution integration and stack testing



Stack Supported | Anode Supported

Techno-economic analysis

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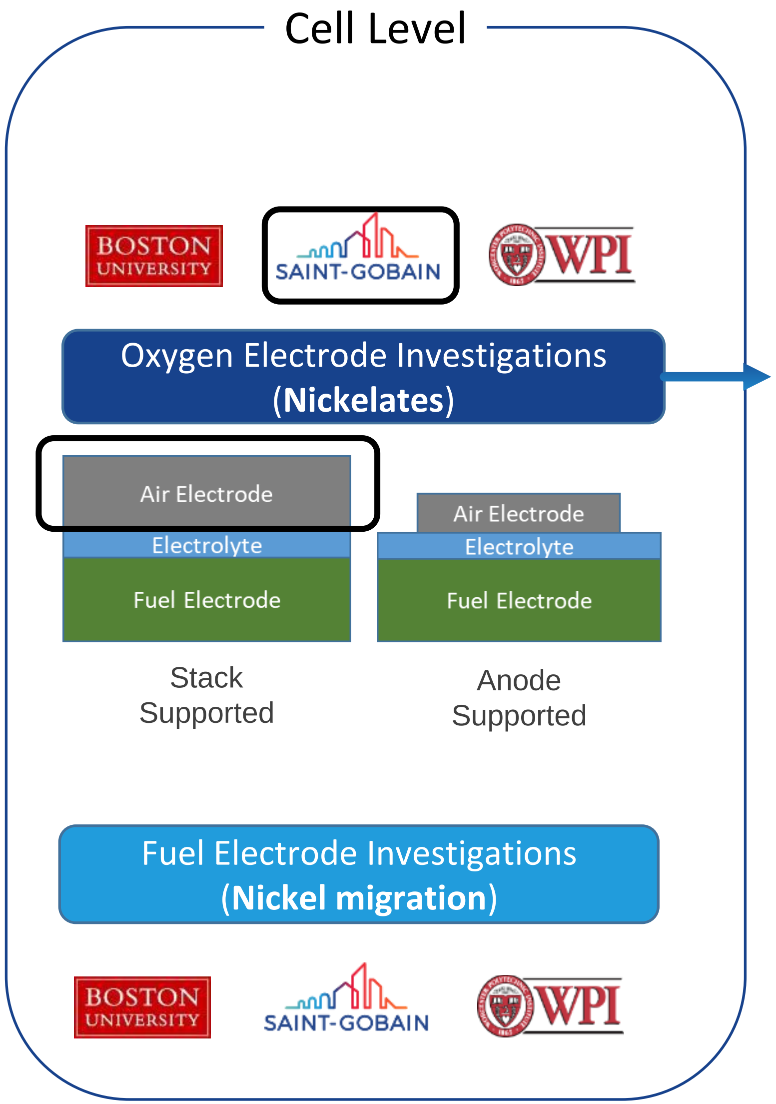
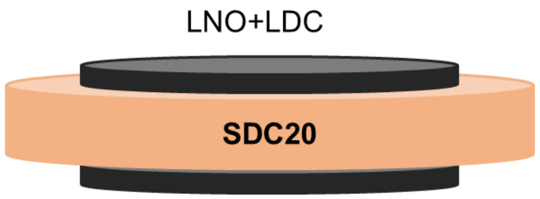
CELL LEVEL MICROSTRUCTURE OPTIMIZATION

AIR ELECTRODE OPTIMIZATION USING NICKELATE MATERIALS



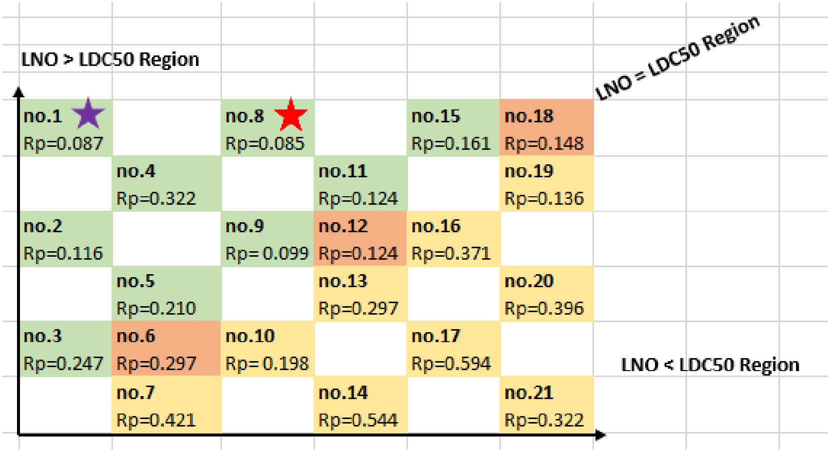
Utilize symmetric cell to iterate particle size ratio between pure ionic and mixed ionic/electronic conductors



Symmetric cell schematic

Initial
Rp 0.24 $\Omega \cdot cm^2$

Optimized
Rp 0.09 $\Omega \cdot cm^2$

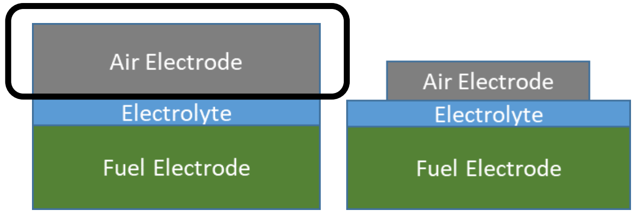


CELL LEVEL PARTICLE SIZE DESIGNED FOR MANUFACTURABILITY

AIR ELECTRODE OPTIMIZATION USING NICKELATE MATERIALS

Cell Level

Oxygen Electrode Investigations
(**Nickelates**)

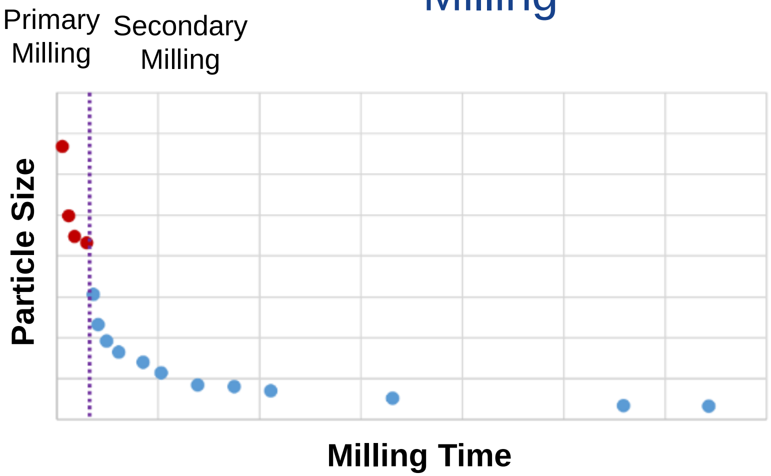


Stack
Supported

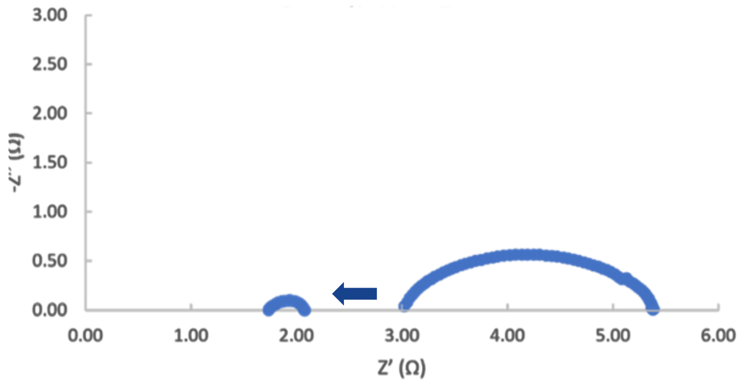
Anode
Supported

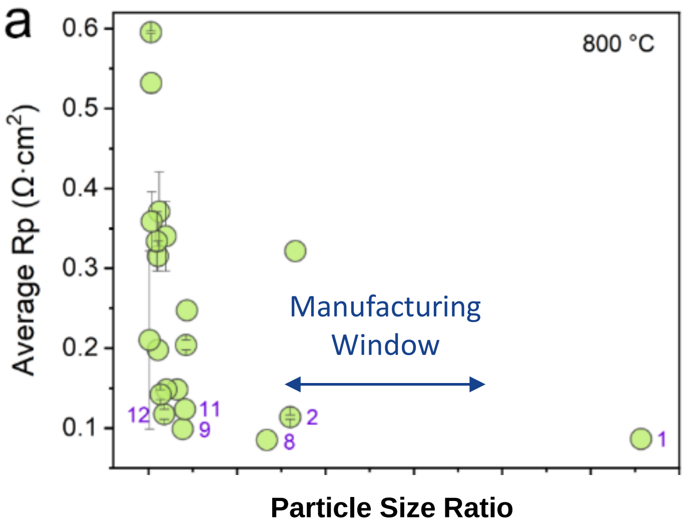
Fuel Electrode Investigations
(**Nickel migration**)

Milling



Symmetric Cell Polarization





Optimized microstructure balancing performance and manufacturability

CELL LEVEL PERFORMANCE AND DURABILITY IMPROVEMENTS

NICKELATE MATERIALS & REDUCED NICKEL MIGRATION

Cell Level

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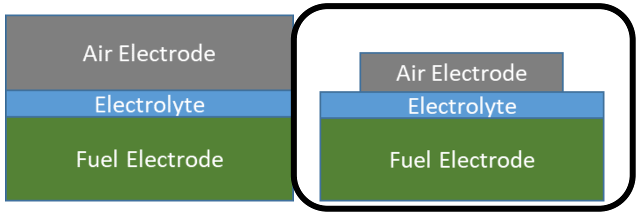
Oxygen Electrode Investigations (Nickelates)



Stack Supported

Anode Supported

Fuel Electrode Investigations (Nickel migration)

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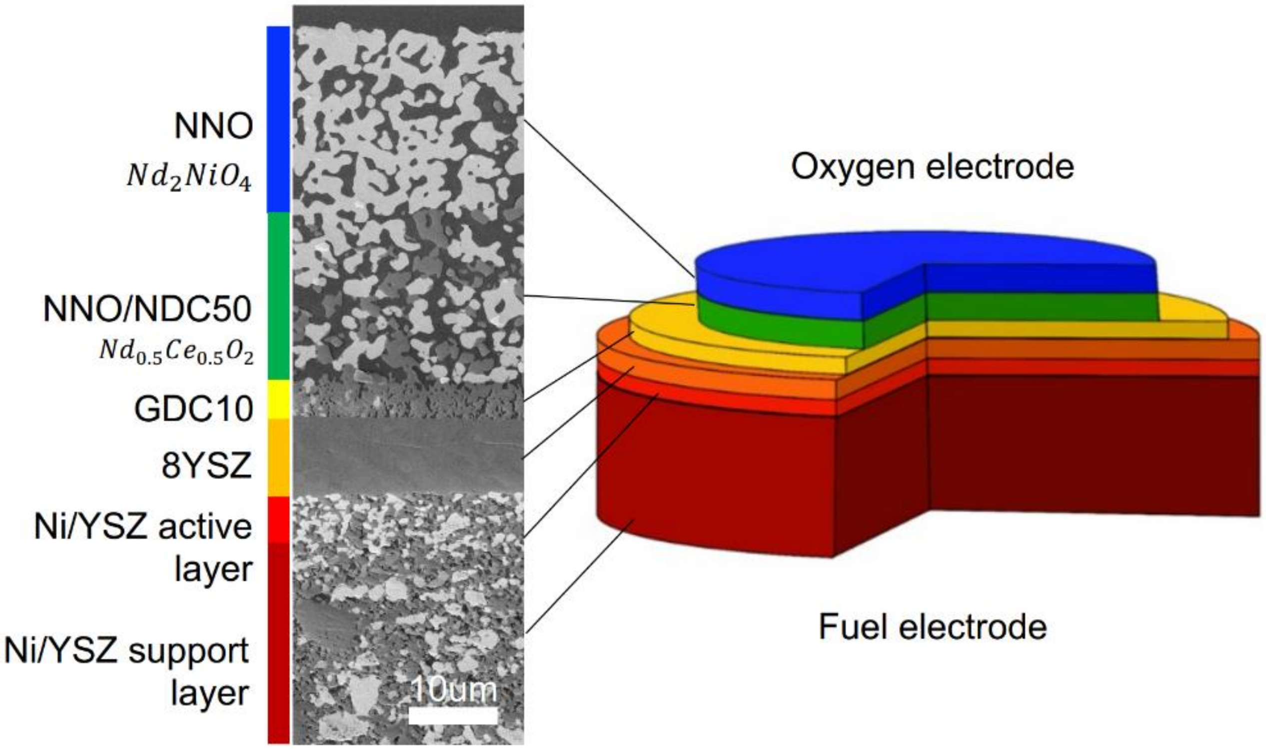
The NNO/NDC50-based RSOC



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CELL LEVEL PERFORMANCE AND DURABILITY IMPROVEMENTS

REDUCED NICKEL MIGRATION THROUGH GDC PINNING

Cell Level

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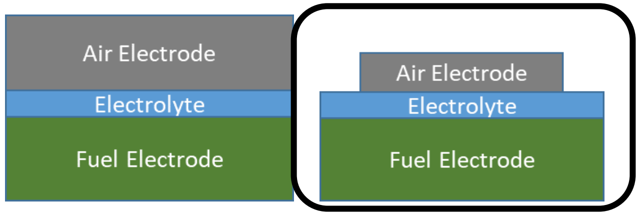
Oxygen Electrode Investigations
(**Nickelates**)



Stack Supported

Anode Supported

Fuel Electrode Investigations
(**Nickel migration**)

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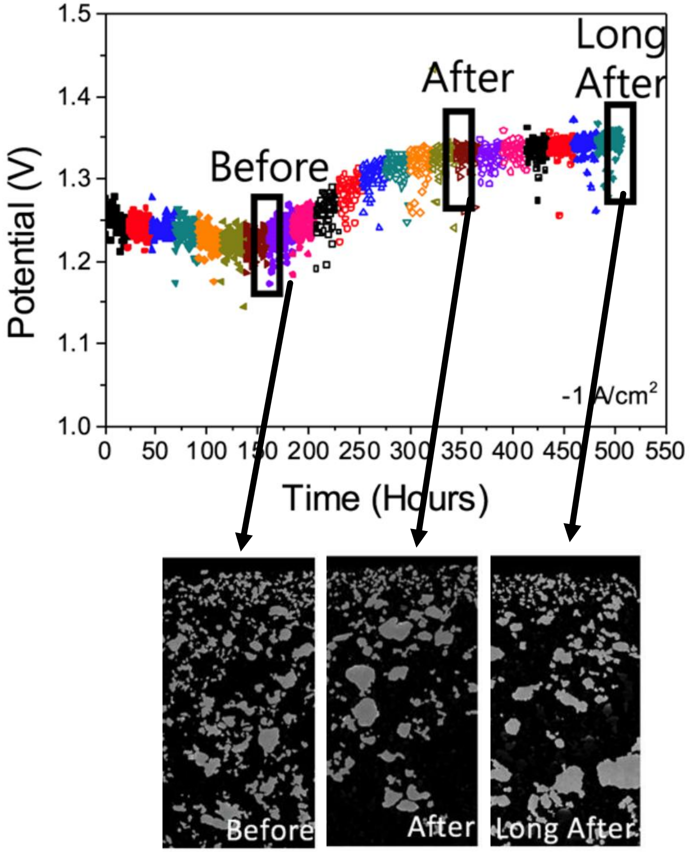
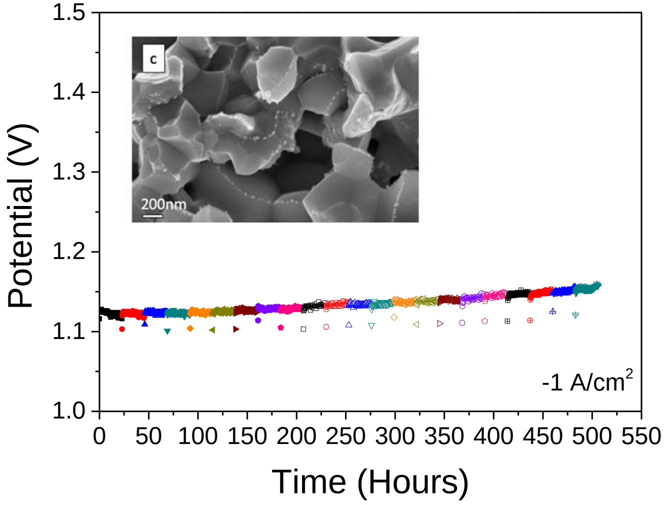
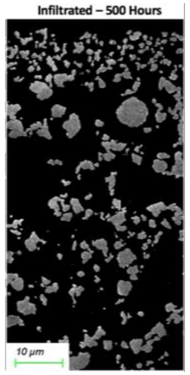
NiO/YSZ electrode without GDC infiltration



Electrochemically Active Regions

NiO/YSZ electrode with GDC infiltration





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CELL LEVEL PERFORMANCE AND DURABILITY IMPROVEMENTS

PERFORMANCE IMPROVEMENT WITH GDC INFILTRATION

Cell Level

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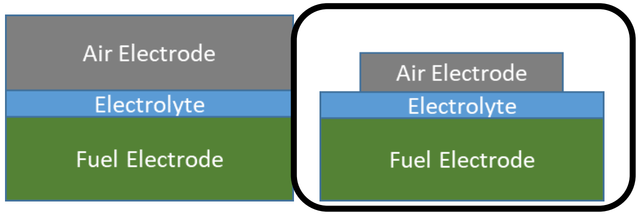
Oxygen Electrode Investigations (Nickelates)



Stack Supported | Anode Supported

Fuel Electrode Investigations (Nickel migration)

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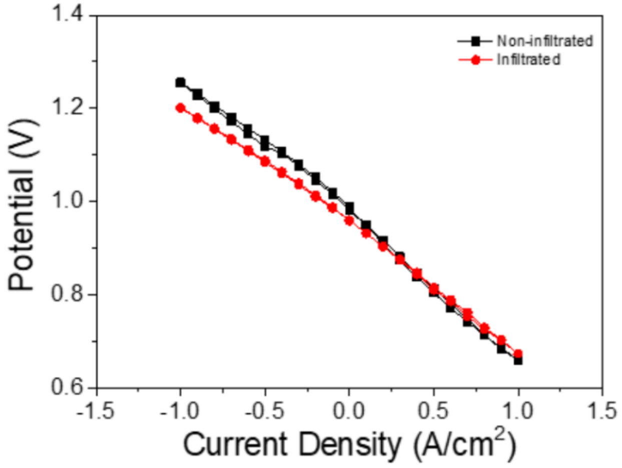
Infiltration of GDC into Ni/YSZ structure results in a reduction of both ohmic and polarization resistance

	Ohmic Resistance ($\Omega.cm^2$)	Polarization Resistance ($\Omega.cm^2$)
As sintered	0.17	0.32
Infiltrated	0.11	0.17

Effect is more apparent in electrolysis mode than in fuel cell mode

300 sccm 50% H_2 50% water vapor (Total 600sccm)
1st batch at initial (0hr)



	Non-infiltrated	Infiltrated
0.7V	0.85A/cm²	0.91A/cm²
1.2V	-0.80A/cm²	-1A/cm²

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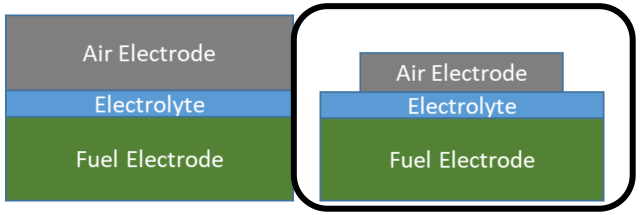
CELL LEVEL PERFORMANCE AND DURABILITY IMPROVEMENTS

PERFORMANCE IMPROVEMENT STABLE IN MODE SWITCHING

Cell Level

Oxygen Electrode Investigations (**Nickelates**)

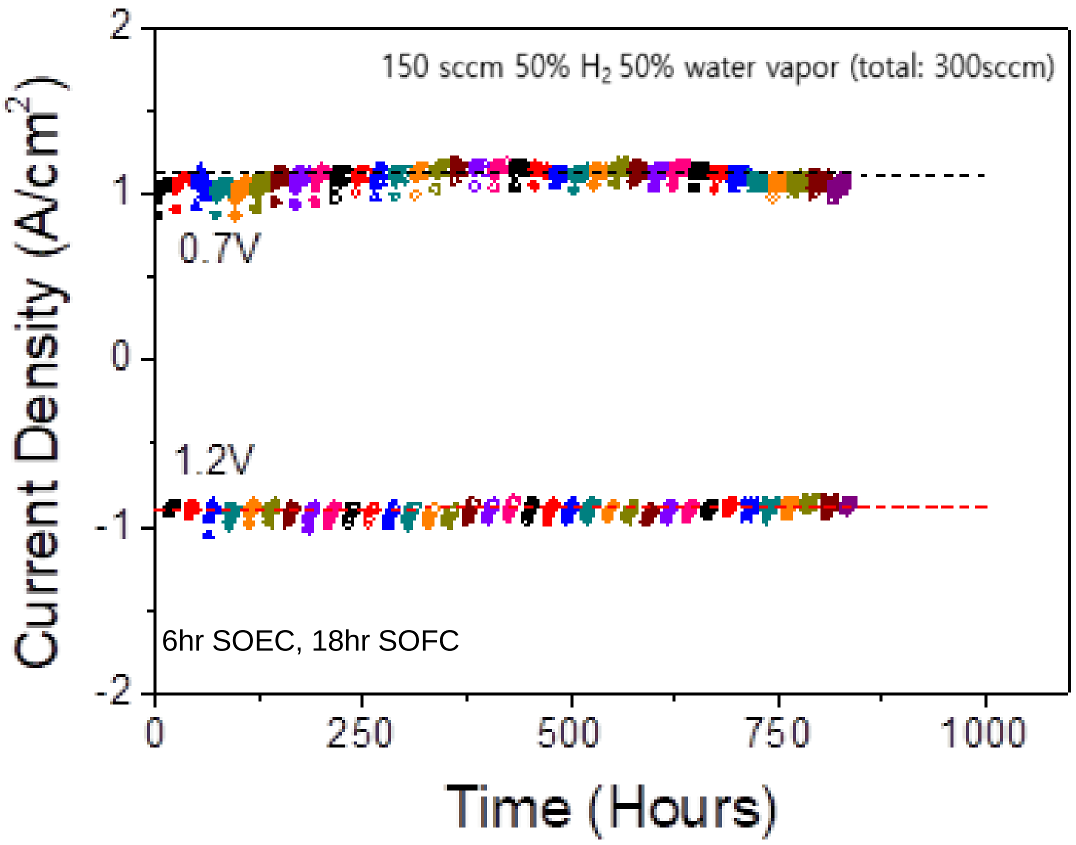


Stack Supported

Anode Supported

Fuel Electrode Investigations (**Nickel migration**)

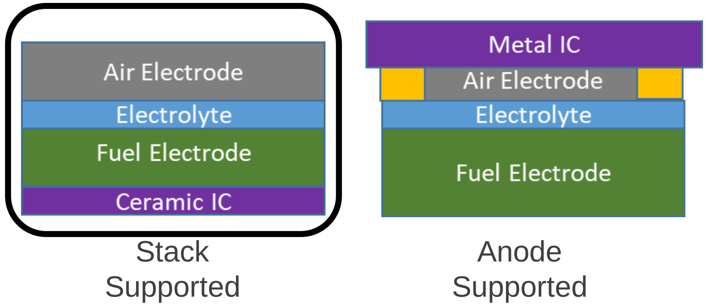
Cell performance quite stable after 800 hrs of continuous cycling between SOFC and SOEC operation modes



CERAMIC INTERCONNECT: AB INITIO CALCULATION OF ELECTRONIC CONDUCTIVITY

Stack Level

Nickelate – Cr interconnect interactions



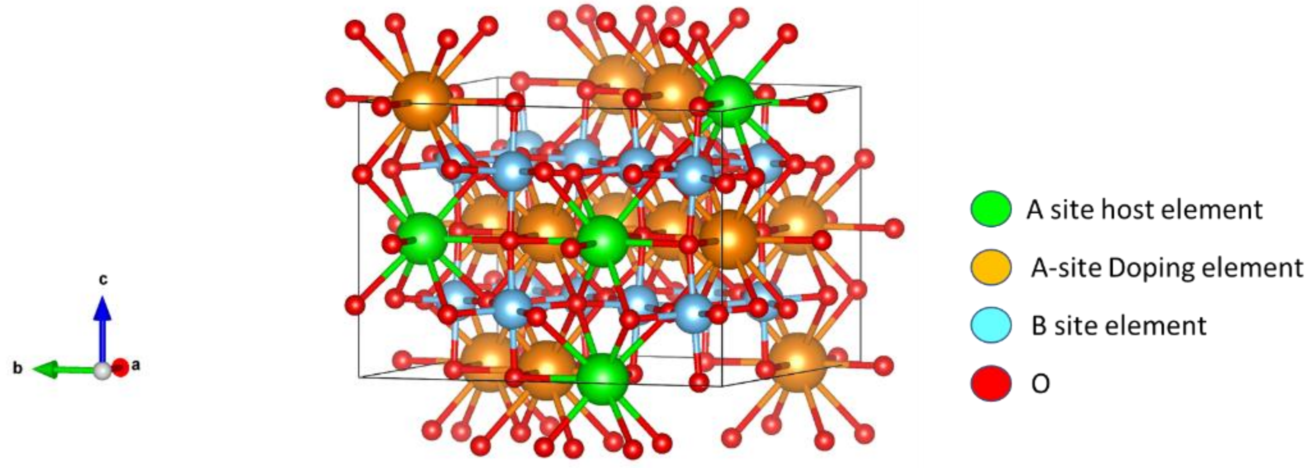
Ceramic IC humidity interactions

Simulation for SG Ceramic Interconnect A (SGCI-A)

- Electronic conductivity vs. T
- Electronic conductivity vs. PO_2
- Electronic conductivity vs. doping element concentration

Simulation for the role of dopants in SG Ceramic Interconnect B (SGCI-B)

- Electronic conductivity of 2-4 doping elements
- Recommendations

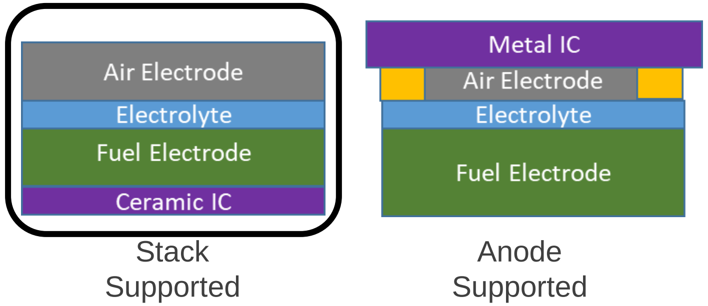


80-atom SQS structures for SGCI-A

AB INITIO CALCULATION OF ELECTRONIC CONDUCTIVITY FOR THE SG CERAMIC INTERCONNECT

Stack Level

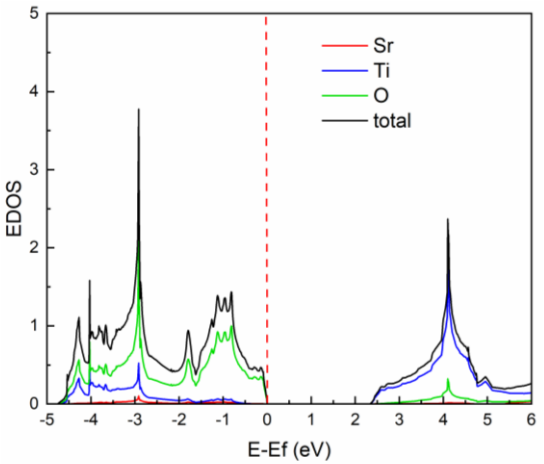
Nickelate – Cr interconnect interactions

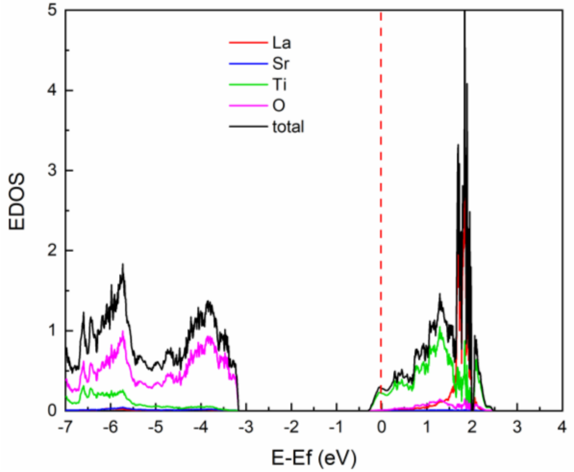


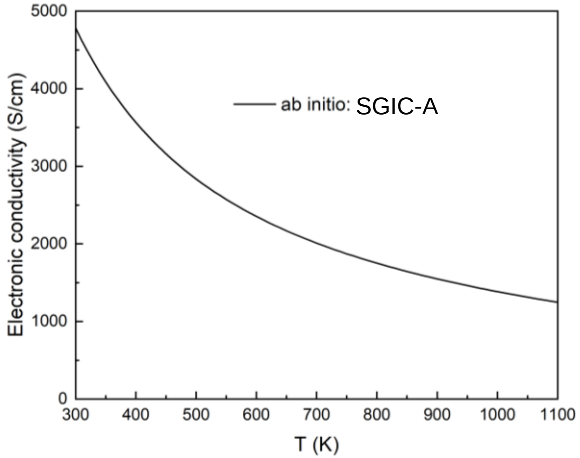
Ceramic IC humidity interactions

Simulation for SG Ceramic Interconnect A (SGCI-A)

- Doping of La into STO results in the closure of the band gap, causing the material to transition into a conductor.
- Under the reducing condition, the electronic conductivity will slightly drop.



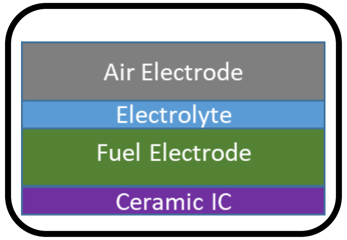




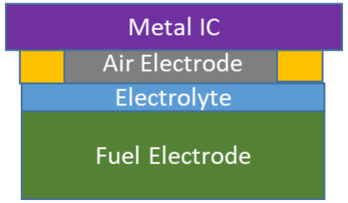
AB INITIO CALCULATION OF ELECTRONIC CONDUCTIVITY FOR THE SG CERAMIC INTERCONNECT

Stack Level

Nickelate – Cr interconnect interactions



Stack Supported



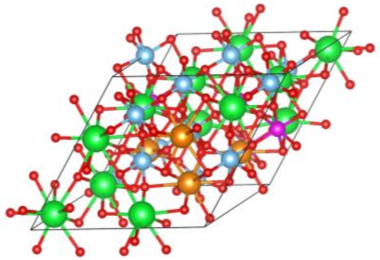
Anode Supported

Ceramic IC humidity interactions

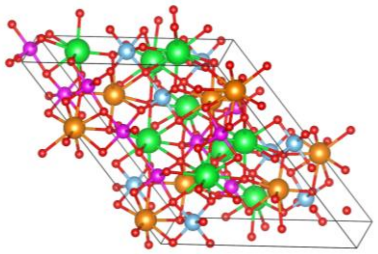
Simulation for SG Ceramic Interconnect B (SGCI-B)

- Modeled both 25% and 50% B-site dopants
- Determined insulating vs semiconducting compositions

SGIC-B1 (25% A and B site dopants)



SGIC-B2 (25% A site dopants and 50% B site dopants)

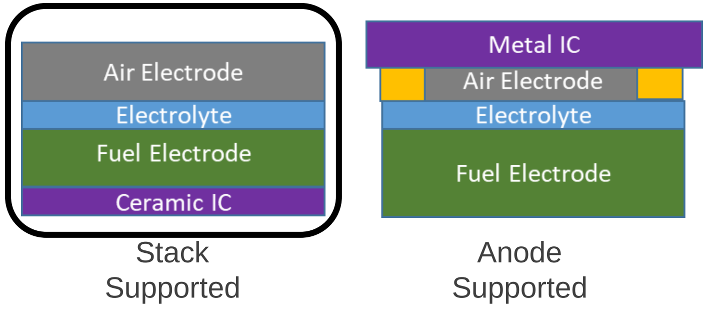


Sturctures	Band gap (eV)	Electronic properties
STO	2.34	Insulator
LST25	none	Conductor
LSTM25	1.18	Insulator
LSTC25	none	Conductor
LSTCF25	0.99	Semi-conductor
LST25_O(reducing condition)	none	Conductor
LSTM25_O(reducing condition)	0.85	Semi-conductor
LSTC25_O(reducing condition)	0.14	Semi-conductor
LSTCF25_O(reducing condition)	0.63	Semi-conductor
LST50	none	Conductor
LSTM50	0.58	Semi-conductor
LSTC50	none	Conductor
LSTF50	0.74	Semi-conductor
LST50_O(reducing condition)	none	Conductor
LSTM50_O(reducing condition)	0.81	Semi-conductor
LSTC50_O(reducing condition)	0.87	Semi-conductor
LSTF50_O(reducing condition)	0.57	Semi-conductor

EXPERIMENTAL MEASUREMENTS ON INTERCONNECT CONDUCTIVITY

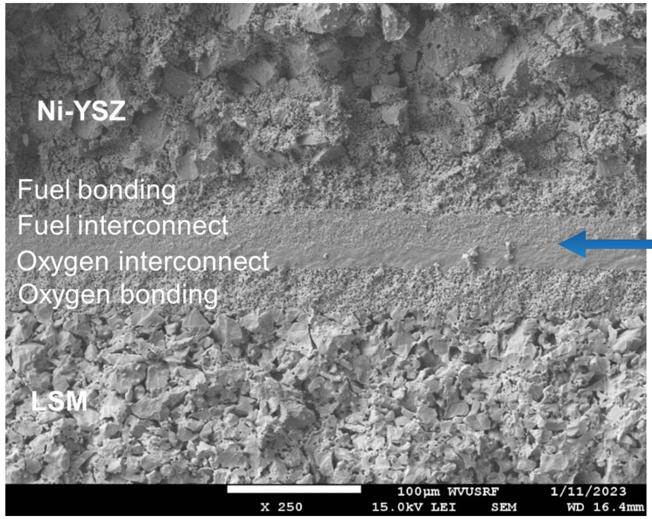
Stack Level

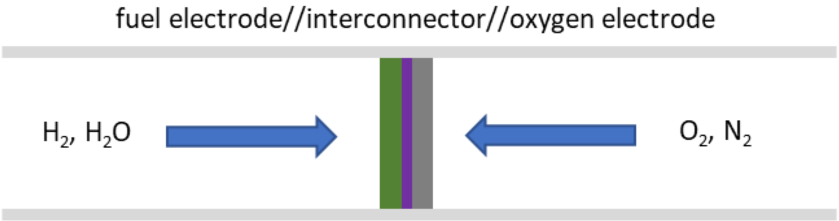
Nickelate – Cr interconnect interactions



Ceramic IC humidity interactions

Mode	Gas to cathode	Gas to anode	Current density (A/cm2)	Duration	Performance (Ωcm²)
SOFC	18 vol.% O_2 balanced by N_2, 300sccm	10vol.% humid H_2, 90sccm H_2+10sccm steam	0.5 (cathode high voltage end)	~2200 h	0.1~0.15
SOFC	18 vol.% O2 balanced by N2, 300sccm	10vol.% humid H2, 90sccm H2+10sccm steam	1 (cathode high voltage end)	~200 h ~600 h	0.05~0.15
SOEC	40 vol.% O2 balanced by N2, 300sccm	20vol.% humid H2, 80sccm H_2+20sccm steam	-0.5 (anode high voltage end)	1000h	0.6~1
SOEC	40 vol.% O2 balanced by N2, 300sccm	20vol.% humid H2, 80sccm H2+20sccm steam	-1 (anode high voltage end)	1000h	0.1~0.3
Reversible SOFC-SOEC	Switching gas between SOFC/SOEC mode every 300h or so	Switching gas between SOFC/SOEC mode	0.5 switch to -0.5 accompanying the gas change	~2200h	0.1~0.25
Reversible SOFC-SOEC	Switching gas between SOFC/SOEC mode every 300h or so	Switching gas between SOFC/SOEC mode	1 switch to -1 accompanying the gas change	~1200h	0.05~0.1
Reversible SOFC-SOEC	Switching gas between SOFC/SOEC mode every 300h or so	Switching gas between SOFC/SOEC mode	0.3 switch to -0.3 accompanying the gas change	~1800 h	0.07~0.1
SOFC (2nd gen interconnect)	**18 vol.% O_2 balanced by N_2, 300sccm**	**3vol.% humid H2, 97sccm H2+3sccm steam**	**0.3 (cathode high voltage end)**	**~1000 h**	**0.03~0.04**
SOEC(2nd gen interconnect)	**40 vol.% O2 balanced by N2, 300sccm**	**40vol.% humid H2, 90sccm H2+10sccm steam**	**-0.3 (anode high voltage end)**	**~1000 h**	**0.03~0.04**



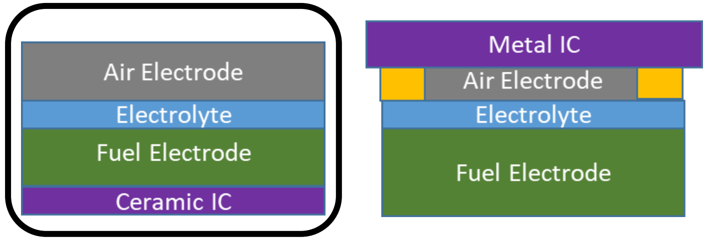


Operated ceramic interconnect in SOFC, SOEC and rSOC modes

EXPERIMENTAL MEASUREMENTS ON INTERCONNECT CONDUCTIVITY

Stack Level

Nickelate – Cr interconnect interactions



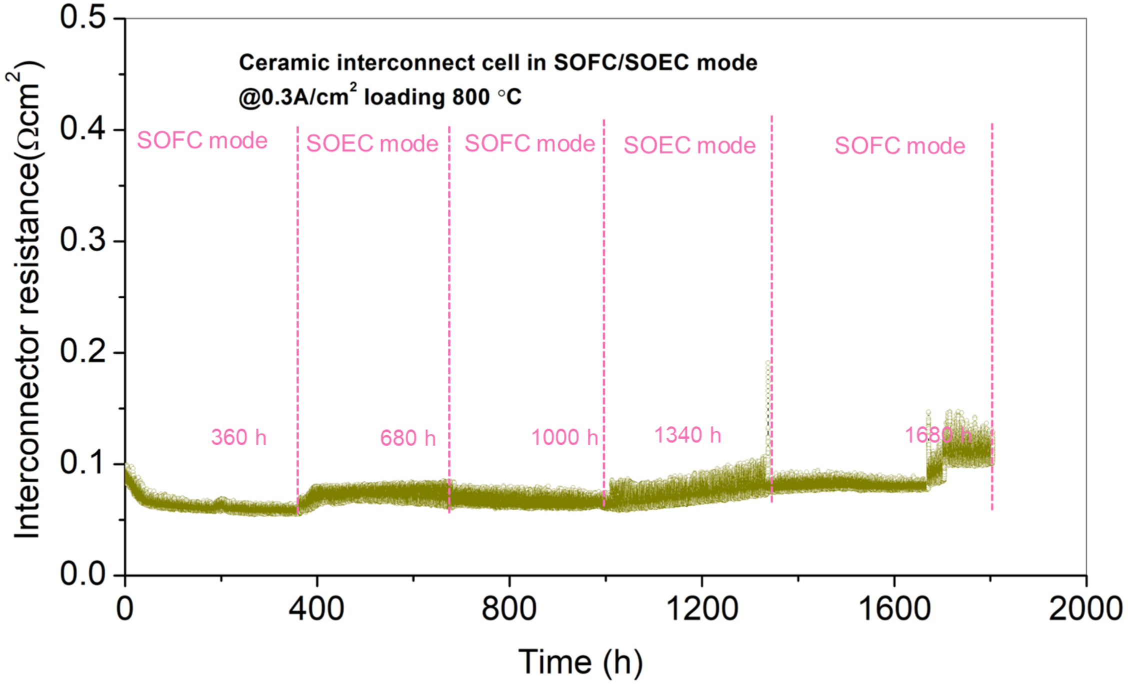
Stack Supported

Anode Supported

Ceramic IC humidity interactions

Example ohmic resistance response to switching mode operation

- Expected small changes in resistance due to changing gas conditions
- Degradation mainly took place in SOEC mode
- Generally stable operation over 1600 hrs
- Resistance value small compared to total resistance of the cell



ENABLING HIGH VOLUME STACK PRODUCTION

ROLL TO ROLL SUBCOMPONENT FABRICATION OF CONSISTENT, THIN LAYERS

Scale Up

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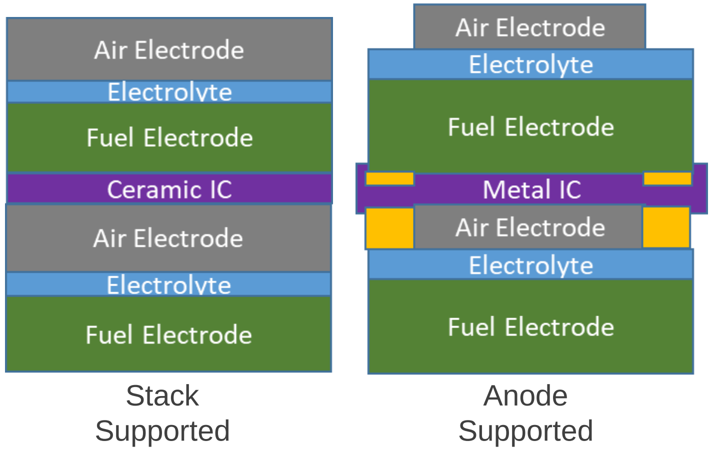
Solution integration and stack testing



Techno-economic analysis

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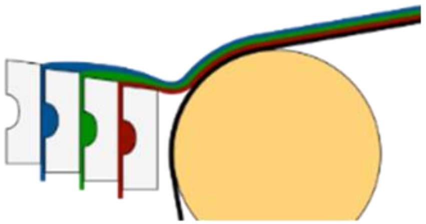
Simultaneous, multi-layer casting is being evaluated to scale co-sintered cell design.

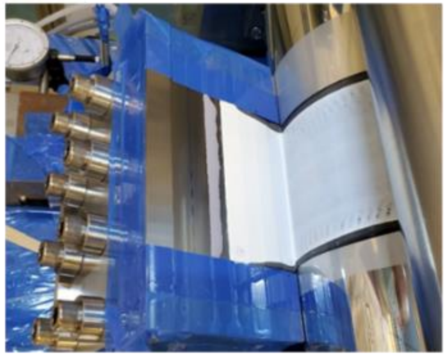
- Multiple ceramic slurries are layered onto a substrate simultaneously during casting.
- Vastly improves quality and efficiency of casting process.
- This method will be used to prove scalability of all-ceramic stack design and provide samples to partner nodes.
- LNO-containing layers will be included as a part of this strategy as soon as is possible.

Simultaneous Multilayer Coating Development



Development Results

- Modification of slurry properties
- Very thin barrier layer possible
- Elimination of punching, stacking, lamination
- Sharp interfaces maintained
- Improved interface integrity

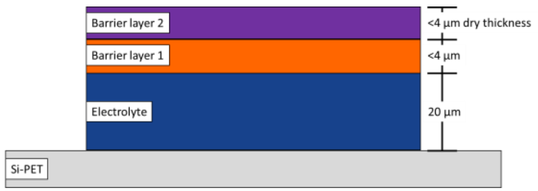


SUCCESSFUL SIMULTANEOUS CASTING

Trial results – excellent control of film homogeneity and microstructure

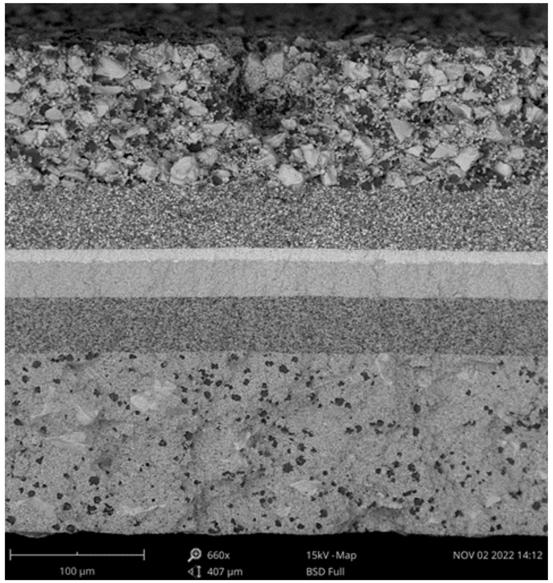
- Stable coating – good separation of 3 layers, smooth coating
- Confirmation of fluid handling approach and workflow strategy
- Layer thickness & architecture were on target
- High quality interfaces and degree of uniformity

Target Design

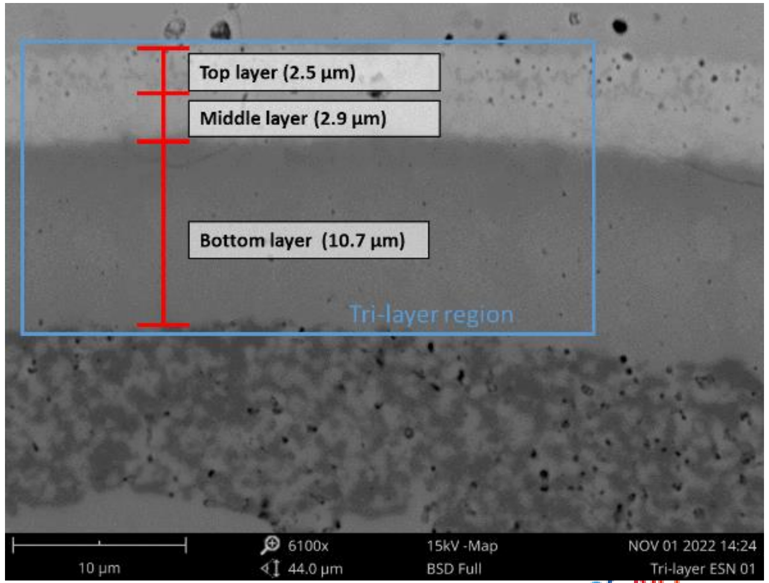


Multilayer Wet Coating

Laminated Green Structure

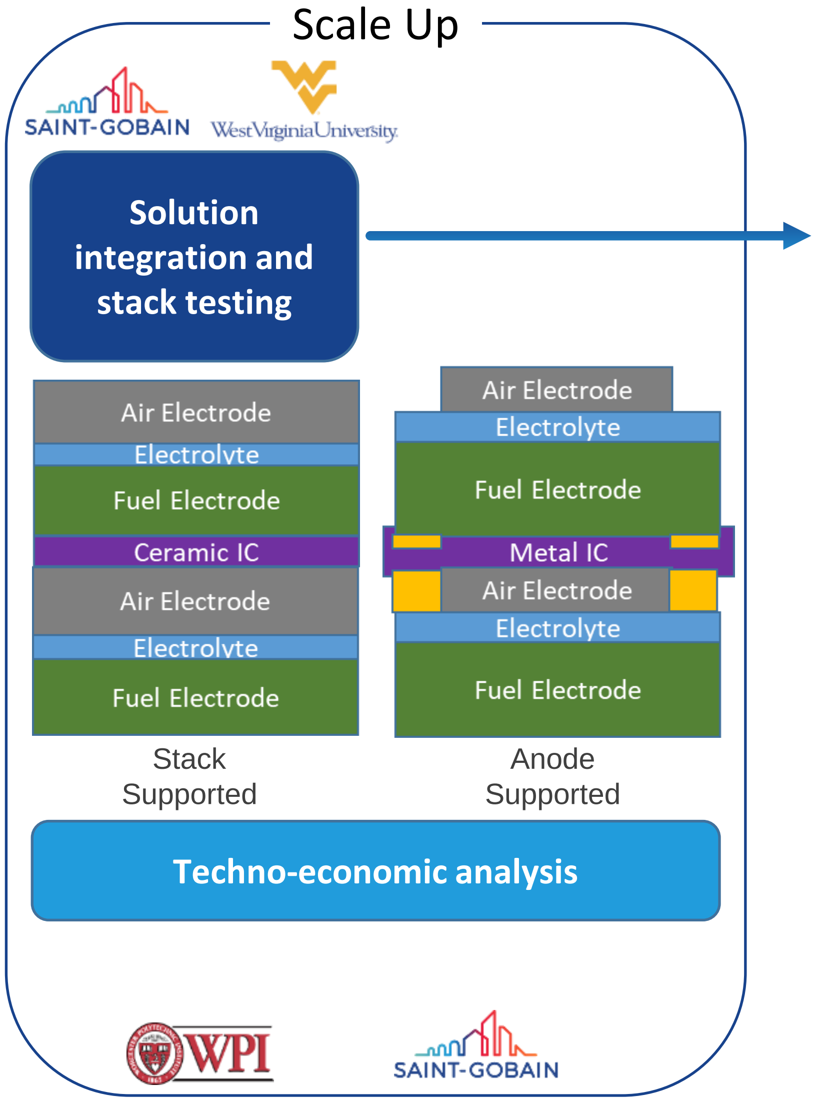


Final Sintered Microstructure

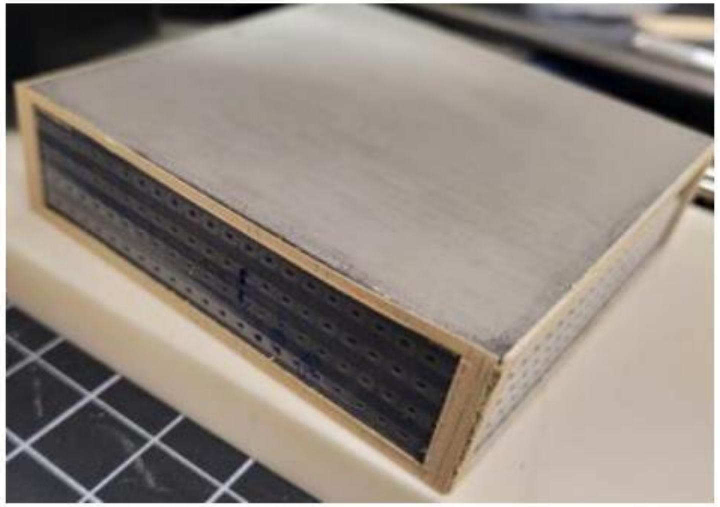


STACK TESTING

MANIFOLDING 8X8 CM, 4-CELL STACK USING CERAMIC MANIFOLD TO ELIMINATE EFFECT OF CHROME VAPOR

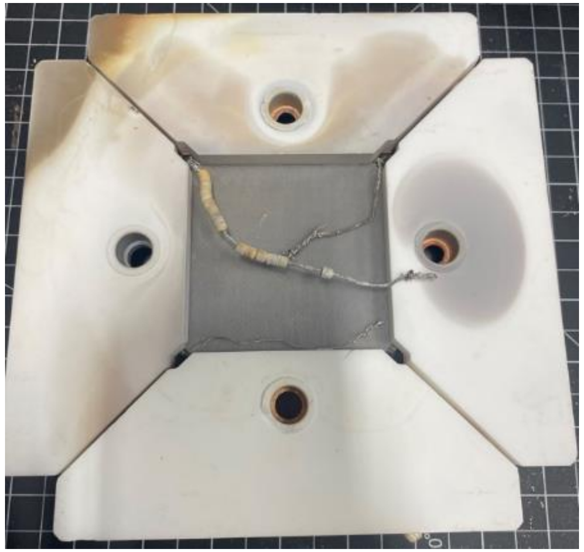


Co-sintered All-Ceramic Stack



- Stack is planarized and glass sealed before manifolding

Manifolded Stack

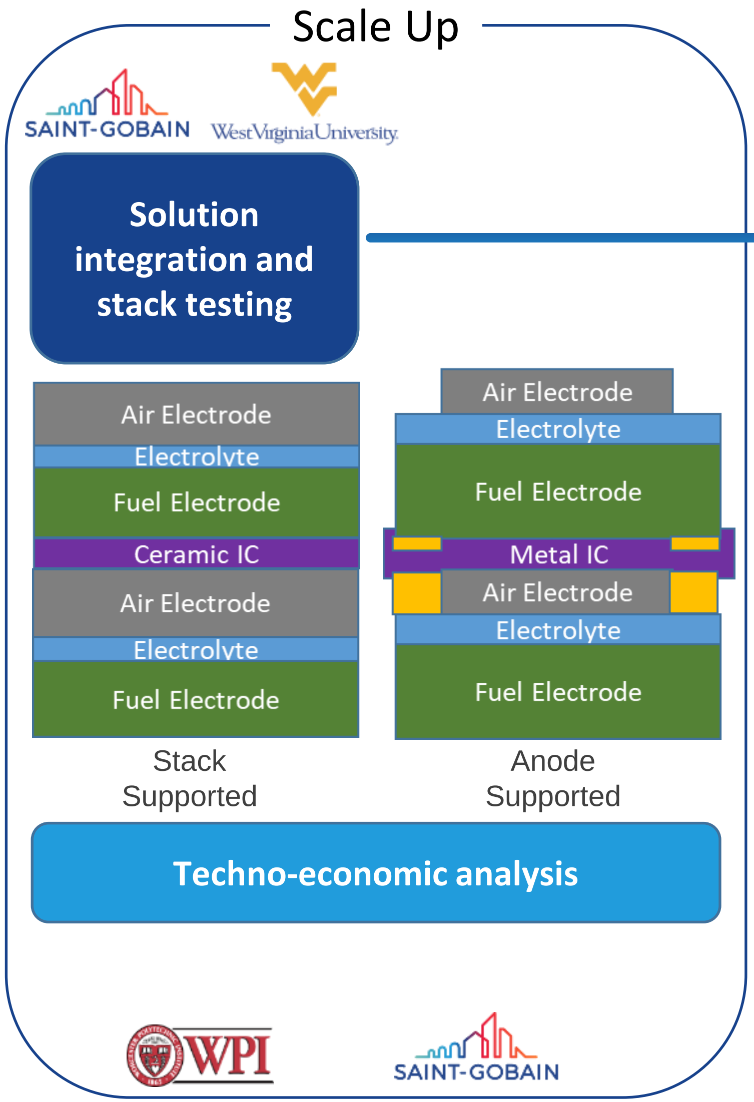


- Placed in manifold with gaskets, platinum mesh, and sapphire plate
- Ceramic hardware used to secure and deliver gas streams

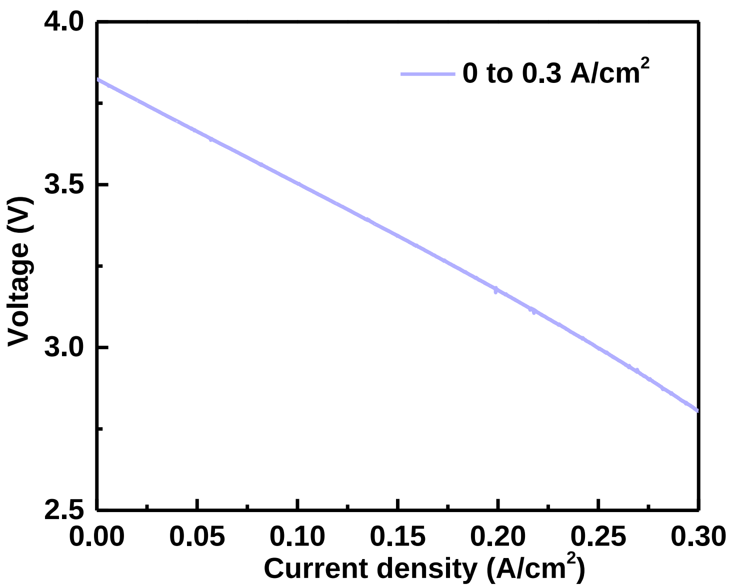
SAINT-GOBAIN

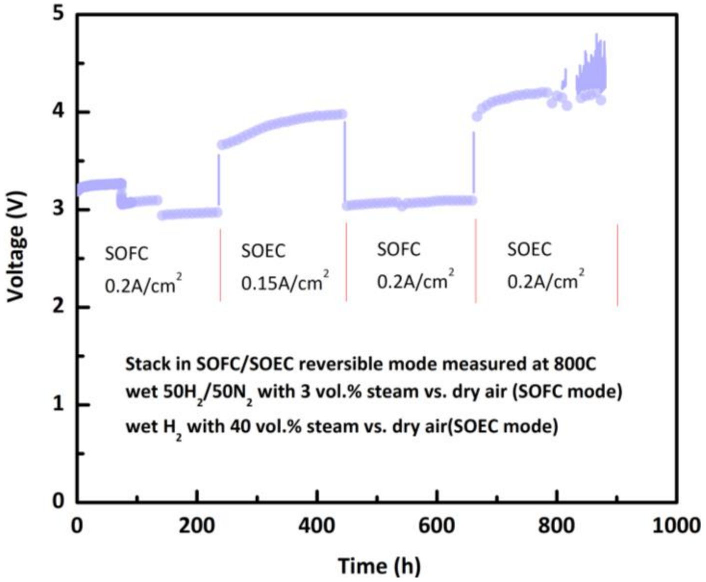
STACK TESTING

RESULTS FROM PREVIOUS GENERATION STACK



- OCV was a little lower than theoretical at 3.83V, sealing imperfection
- I-V curve scanning from 0-0.3 A/cm2, as expected performance based on button cells
- Performance slightly improves during SOFC mode but degrades a little bit under SOEC mode.

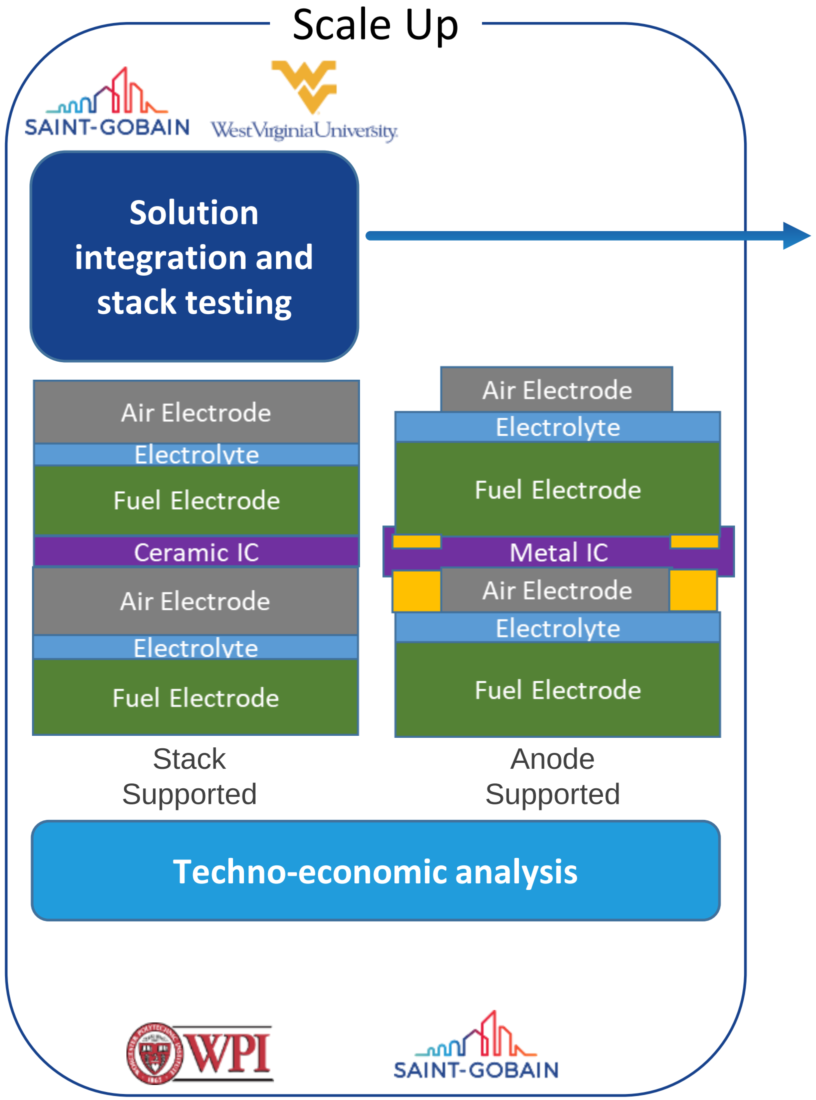


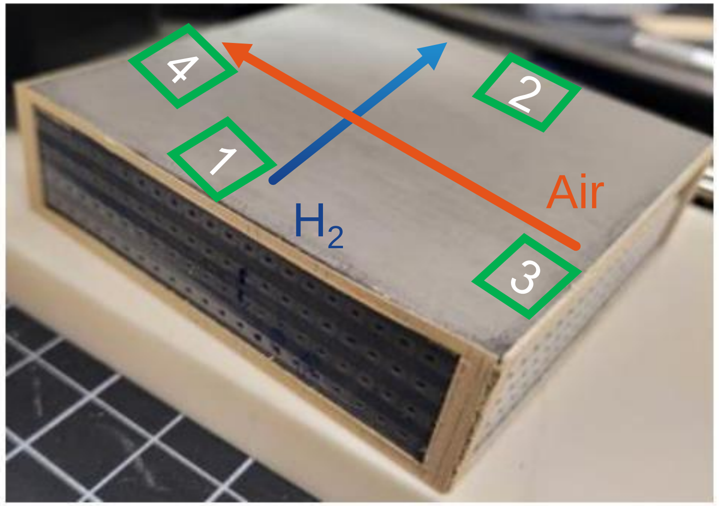


SAINT-GOBAIN

STACK TESTING

SEM ANALYSIS POST TESTING, 1400 HRS

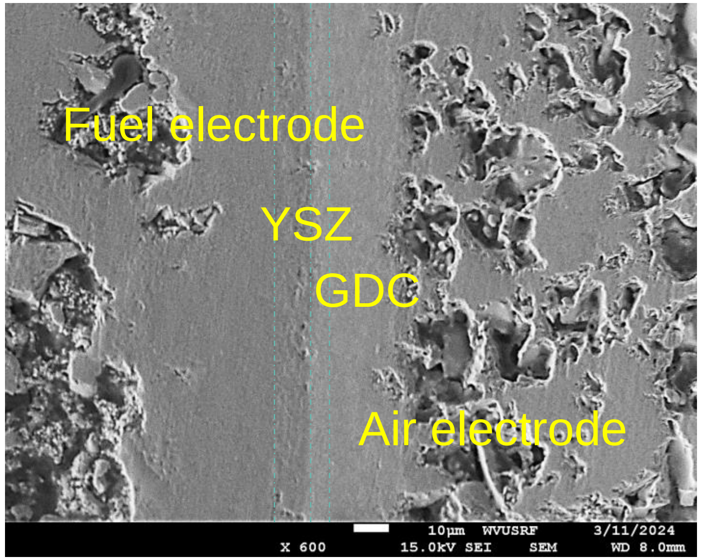




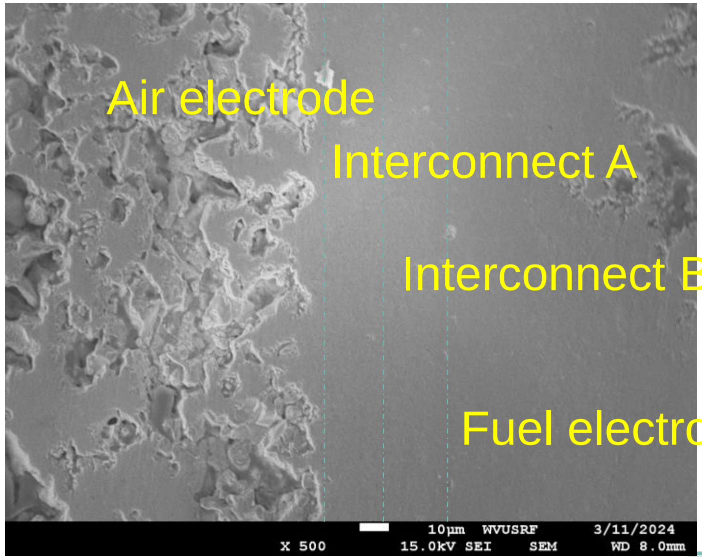
Four locations observed corresponding to extreme gas/current density

- No locational effects noticed
- No cracking or delamination detected at the electrolyte or interconnect

electrolyte interfaces



interconnect interfaces



SAINT-GOBAIN

SUMMARY

DE-FE0031972

Achievements

- Optimized the oxygen electrode particle size ratios resulting in reduced resistance
- Developed a simple technique to quantify microstructural changes due to Ni migration
- Improved performance and durability in mode switching operation
- Developed a robust, first principles model of titinate ceramic interconnect
- Measured effect of high water vapor of SOEC mode operation on ceramic interconnect
- Developed a simultaneous multi-layer roll to roll process enabling thin and low-cost production
- Produced 4-cell stacks and tested performance in mode switching operation

Next Steps

- Produce full cells with optimized particle size distribution
- Move optimized air electrode microstructure to stack level production
- Test optimized stack in mode switching
- Utilize performance data for system level performance and cost modeling