Electrodeposited Mn-Co Alloy Coating For SOFC Interconnects

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Overall Objective

Develop, optimize & validate an inexpensive manufacturing process for coating metallic SOFC interconnects with Co and Mn.

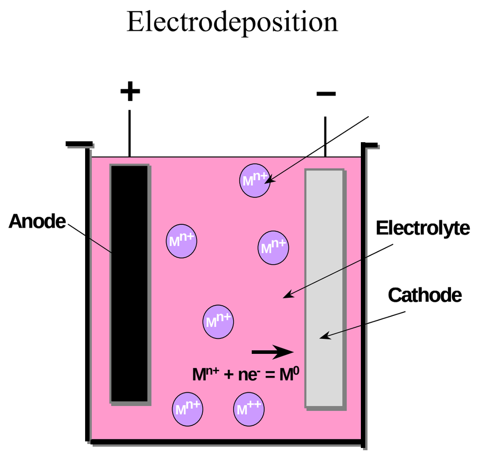
Introduction

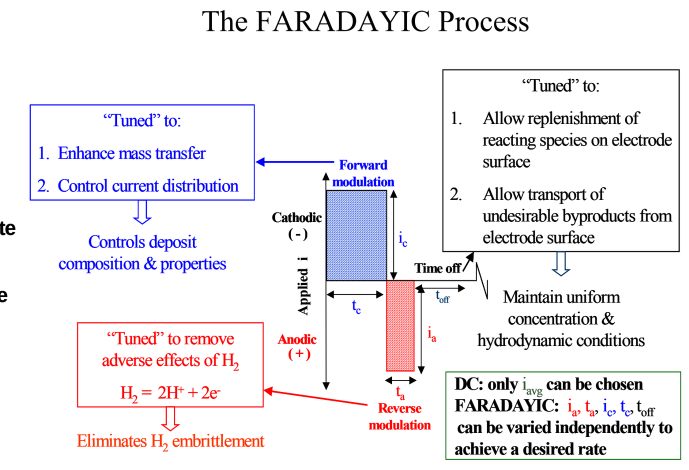
Reducing SOFC operating temperatures below 1000ºC has permitted less resistive and expensive ferritic stainless steel interconnects to replace ceramic materials. However, even specially developed ferritic alloys operated at elevated temperatures for lengthy periods of time form a chromia scale that increases the interconnect resistance and results in chrome diffusion from the interconnect to the cathode that causes a reduction in cathode performance. One attractive method to resolve the chromia scale growth and diffusion issues is to electrodeposit a Mn-Co alloy coating onto the interconnect surface and subsequently oxidize it to $(Mn,Co)_3O_4$.

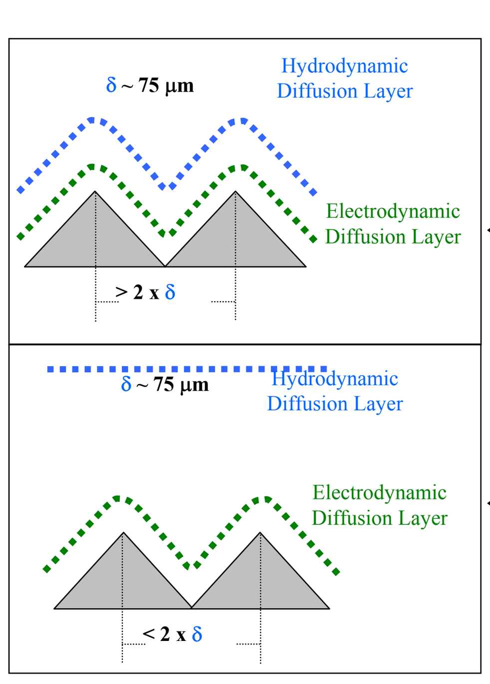
Under funding from the Department of Energy, Faraday Technology and WVU demonstrated that the electrodeposition process can produce Mn-Co alloy coatings with adequate adhesion after 2000 hrs at 850ºC for specific compositional ranges and that a 3 µm coating is sufficient to minimize chrome diffusion to the surface after 500 hrs at 800°C in air. Furthermore, a preliminary economic assessment, based on a batch manufacturing process, suggests that the pulse/pulse reverse electrodeposition technology can meet the Department of Energy's high volume target of 1,600,000 plates per annum at a cost of ~$1.23 per 25 cm x 25 cm coated interconnect.

Approach

The FARADAYIC Electrodeposition process







The appropriate waveform can alter the thickness of the pulsating diffusion layer and effectively focus or defocus the current distribution to create non-uniform or uniform deposition respectively.

Macroprofile: Diffusion layer tends to follow the surface contour. Mass transport control results in a uniform current distribution or a conformal deposit during deposition.

Microprofile: Diffusion layer thickness surface roughness. Mass transport control results in a non-uniform current distribution.

The FARADAYIC Electrodeposition process…

- Enables alloy composition control
- Enables control of coating uniformity for flow field patterns
- Maintains fast processing times to enable high throughput manufacturing
- Is an inexpensive manufacturing process for SOFC interconnect coatings

Milestones

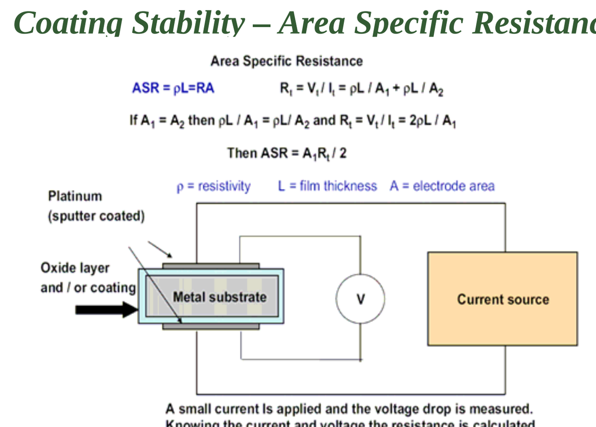
Fiscal Year	Title	Planned Completion	Percent Complete
2011	1. Design/modification of 10" x 10" electrodeposition cell	May 2011	100%
2011	2. Long-term high temperature, thermal evaluation	September 2011	33%
2011	3. Process development for 4"x4" planar interconnects	September 2011	15%
2012	4. Process development for 4"x4" pattern interconnects	June 2012	0%
2012	5. Long-term on-cell performance evaluation	August 2012	0%
2012	6. Qualification/demonstration of IC in single cell test rig	September 2012	0%

Previous Accomplishments

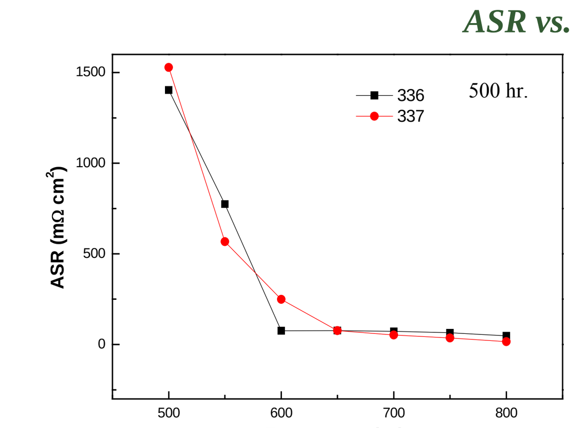
Test Matrix for Samples Undergoing a 500 hour Soak at 800 °C

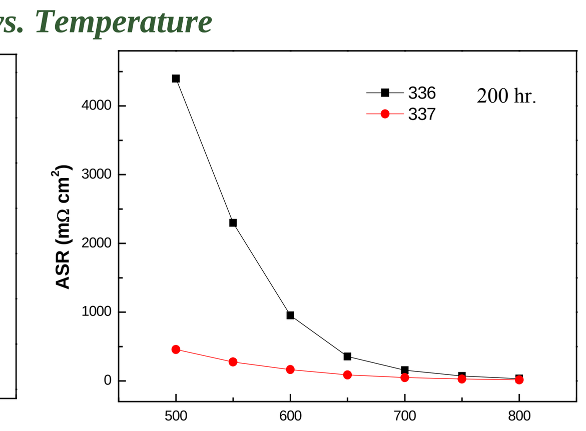
Sample No.	Deposit Thickness (µm)	% Co Composition Before 800 °C Bake	% Composition After 800 °C Bake
332	3	65	40
333	7	65	40
334	10	65	40
335	3	80	85
336	7	80	85
337	10	80	85
338	3	78	57
339	7	78	57
340	10	78	57

Coating Stability – Area Specific Resistance



ASR vs. Temperature

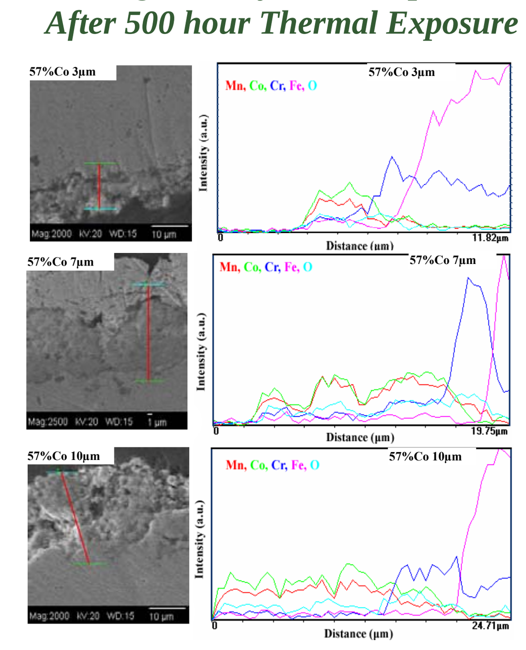




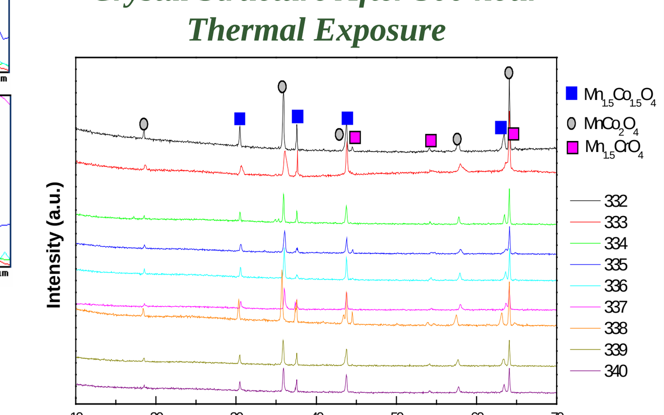
ASR at 800°C

mΩ cm²	100 hr	200 hr	500 hr
3 µm 40% Co	35	57	49
7 µm 40% Co	62	7	32
10 µm 40% Co	22	-	36
3 µm 85% Co	31	75	20
7 µm 85% Co	59	40	54
10 µm 85% Co	37	23	22
3 µm 57% Co	-	34	26
7 µm 57% Co	-	-	12
10 µm 57% Co	-	-	12

Coating Porosity and Composition After 500 hour Thermal Exposure



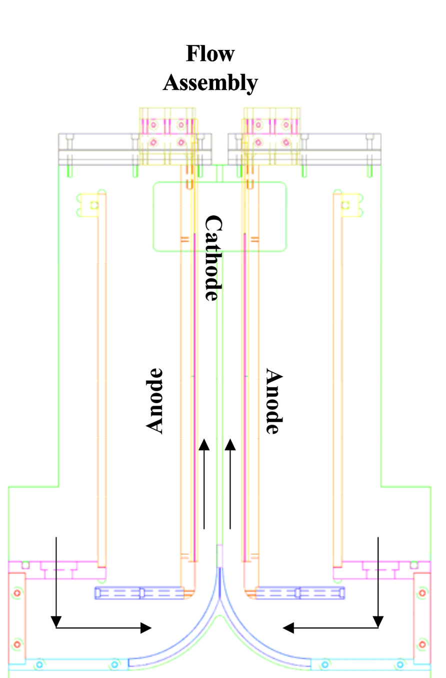
Crystal Structure After 500 hour Thermal Exposure



Processing Equipment

Electrochemical Cell

Based upon Faraday's electrochemical cell design that facilitates uniform flow across the surface of a flat substrate (US patent #7,553,401)



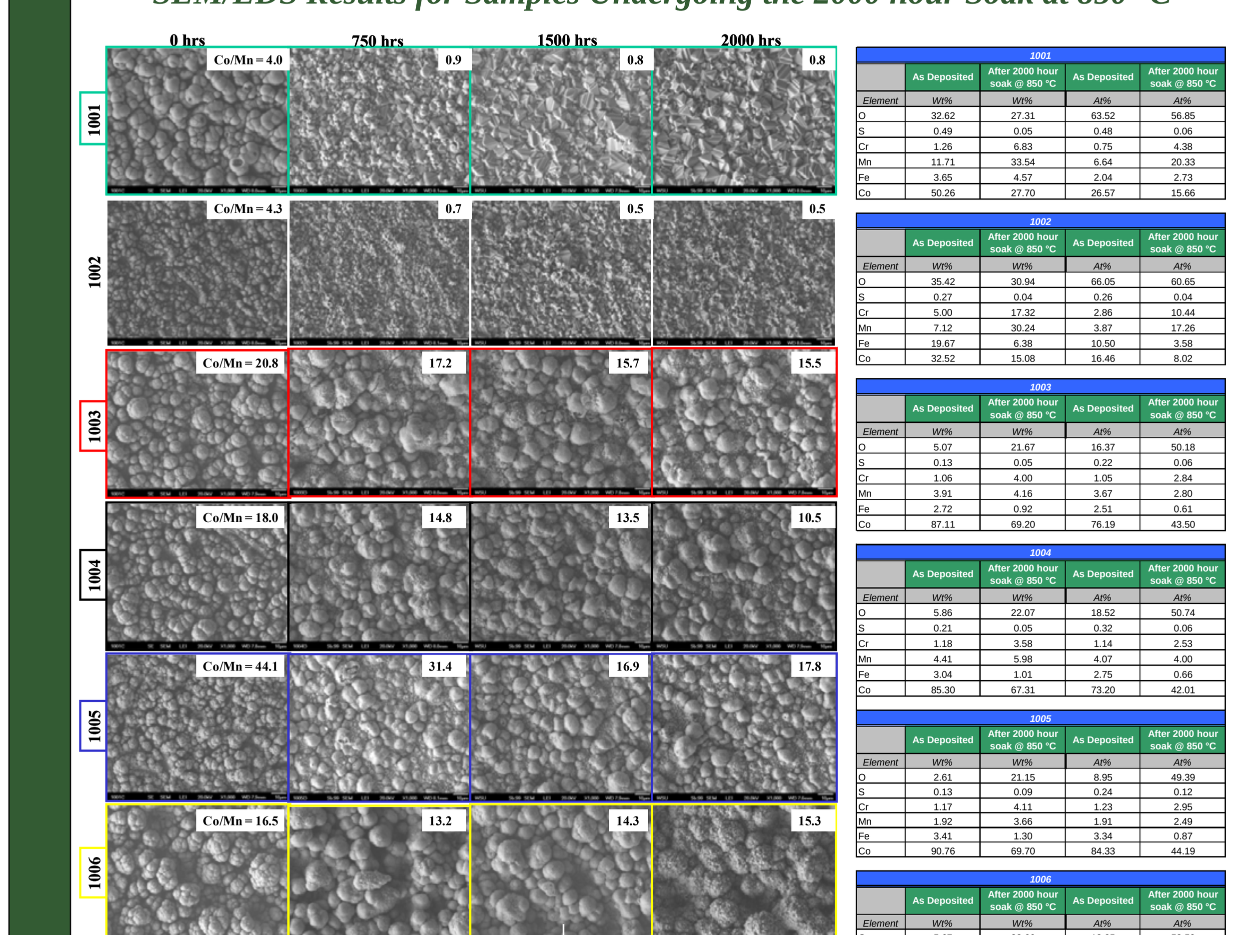
Modified FARADAYIC Electrodeposition Cell for coating patterned interconnect substrates ranging in size from 1"x1" to 10"x10".

Results

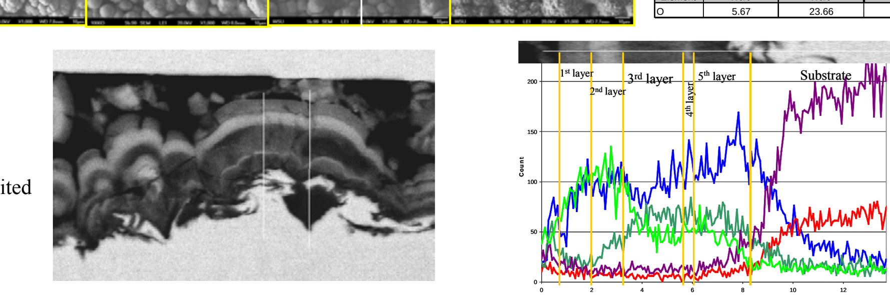
Test Matrix for Samples Undergoing a 2000 hour Soak at 850 °C

Trial No.	Temp (°C)	Current density (mA cm^{-2})	Forward On-time (mS)	Reverse On-time (mS)	Off-time (mS)	Frequency (Hz)	Exp't Time (min)
1001	30	200	9	N/A	1	100	8.8
1002	30	150	9.7	0.3	N/A	100	7.7
1003	50	150	9.7	0.3	N/A	100	8.1
1004	50	200	9	0.3	0.7	100	5.6
1005	70	150	9	N/A	1	100	5.2
1006	50	200	9.7	0.3	N/A	100	10.6

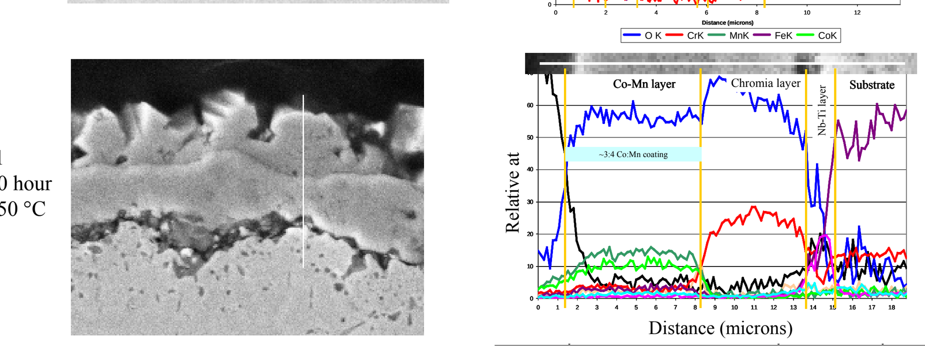
SEM/EDS Results for Samples Undergoing the 2000 hour Soak at 850 °C



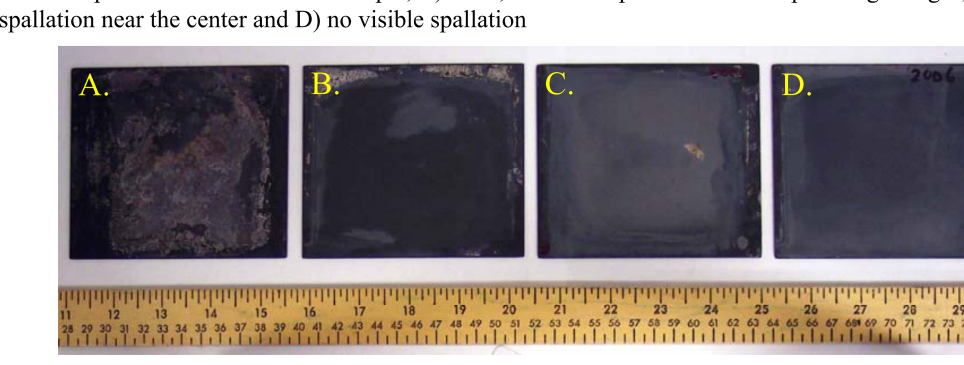
1001 As Deposited



1001 After 2000 hour soak at 850 °C

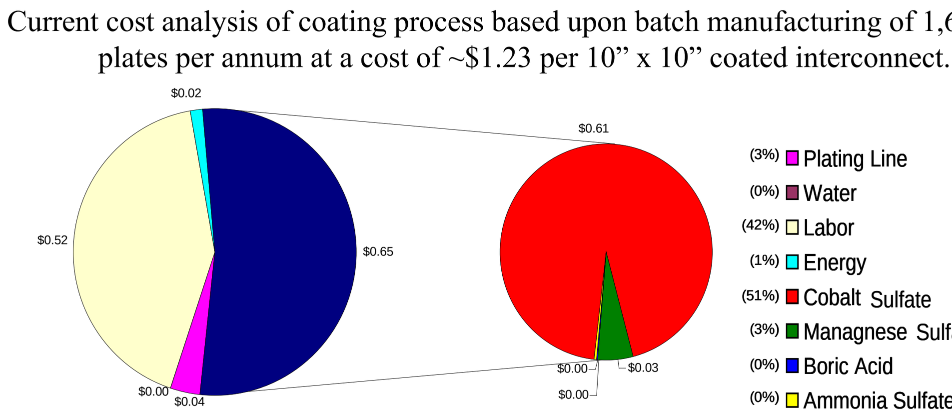


Photographs of 4"x4" planar interconnects electrodeposited with Mn-Co alloy coatings exhibiting varying degrees of spallation after undergoing a 72 hour post-deposition thermal treatment at 850 °C. A) 2002, extreme spallation over the entire sample, B) 2005, moderate spallation at the top and right edges, C) low spallation near the center and D) no visible spallation



Economic Analysis

Current cost analysis of coating process based upon batch manufacturing of 1,600,000 plates per annum at a cost of ~$1.23 per 10" x 10" coated interconnect.



Conclusions/Future Work

Conclusions

- FARADAYIC Process allows for non-line-of-sight deposition of a wide range of compositions and surface structures using a single plating bath
- Initial ASR and crystallinity analysis showed that the as-deposited thickness/composition had little effect on performance after a 500 hr heat cycle
- 3µm thickness is capable of minimizing Cr diffusion for 500 hr testing
- Based on batch manufacturing, the DOE's high volume target of 1,600,000 plates per annum at a cost of ~$1.23 per 25 x 25 cm interconnect

Future Work

- Determine plating parameters effect on chromium and oxygen diffusion
- Determine plate uniformity over large area flat T441 substrates
- Verify dual-sided plating flexibility
- Coat pattern interconnect
  – Demonstrate coating uniformity and composition
- Testing in single cell and short stack SOFC systems

Acknowledgements

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